REMARKS

The Office Action mailed July 26, 2002, has been received and reviewed. Claims 1 through 9 are currently pending in the application. Claims 1 through 9 stand rejected. Applicants have amended claims 3, 6, 7 and 8, added new claims 10 through 14, and respectfully request reconsideration of the application as amended herein.

Double Patenting Rejection Based on U.S. Patent No. 6,008,538

Claims 1 and 2 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,008,538. In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a Terminal Disclaimer to obviate the double patenting rejection in compliance with 37 CFR §1.321 (b) and (c). Applicants' filing of the Terminal Disclaimer should not be construed as acquiescence of the Examiner's obviousness-type double patenting rejection. Enclosed are the Terminal Disclaimer and required fee.

35 U.S.C. § 112 Claim Rejections

Claim 7 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended claim 7 to delete the term "traffic control" to overcome the rejection.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,502,333 to Bertin et al.

Claims 3 through 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bertin et al., U.S. Patent No. 5,502,333. Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants have reviewed the Bertin et al. reference, and note that the reference fails to disclose a substrate "having a plurality of memory chips *individually* mounted thereon" as presently claimed in claim 3. A review of the reference appears to reveal that all of the embodiments incorporate stacks of chips in one form or another, rather than a design wherein each memory chip is individually mounted to a substrate. The inclusion of a "spare" chip in the stack as disclosed or "spare" cells within chips in the stack which may be addressed and thus enabled should defective memory be detected, is thus markedly different than the present invention.

In the present invention, a memory module is fabricated with the *capability* of adding memory to replace memory found to be defective, but *not* additional memory in the first instance, just in case there defective memory is exhibited upon testing. Instead, there are "one or more" additional locations on the substrate "configured to incorporate functional memory of one or more additional chips disposed at said one or more additional *individual* locations *on said substrate*" (Emphasis added). Thus, in the present invention, no "spare" chips or memory are added to the memory module unless and until some memory of the plurality of chips initially comprising the memory module are found to be defective. Bertin et al., as a result of the designs of the various embodiments thereof, does not appear to disclose "one or more additional individual locations on said substrate" configured to receive additional one or more additional chips. Instead, Bertin et al. builds in some additional memory and completes fabrication of the module, relying on detection of nonfunctional memory and rerouting using logic to redundant memory already built in to the module in anticipation of some failures. Accordingly, Bertin et al. does not anticipate claim 3, and the rejection should be withdrawn.

Claim 4 is allowable as depending from claim 3, and further because Bertin et al. fails to *inherently* teach that its additional chip or other spare memory cells are in an amount equivalent to or greater than nonfunctional memory which *may* be exhibited upon testing of the stacked chips of the module. Accordingly, Bertin et al. does not anticipate claim 4, and the rejection should be withdrawn.

Claims 5, 6 and 7 are respectively allowable as depending from claims 3 and 4.

Claim 6 is also allowable with respect to Bertin et al. as the reference fails to disclose the use of two different memory chips having 1) different memory capacity and 2) placed at different additional individual locations on a substrate.

Claim 8 is allowable as Bertin et al. fails to disclose a plurality of memory chips individually mounted to a substrate. Further, Bertin et al. does not *inherently* teach a module stack wherein the memory chips collectively exhibit an amount of nonfunctional memory exceeding a memory capacity of any one ship of the plurality, nor does the reference *inherently* teach at least one additional memory chip providing an amount of functional memory equal to or greater than said amount of collective nonfunctional memory exhibited by the other chips. This is because Bertin et al. builds their stacked chip modules incorporating one or more redundant chips in the first instance, the capacity of which redundant chip or chips may be based on "empirical yield data" (Col. 6, lines 29-32). Applicants, on the other hand, by adding chips *after* their module is tested, are enabled to add enough memory to ensure functionality of their module, but not more memory than may be required. Similarly, Bertin et al. may end up with a chip stack module which is inoperative as the one or more redundant memory chips may not provide sufficient memory to make up for the nonfunctional memory of the primary chips of the stack module, since the redundant chip or chips are built in when the stack module is initially fabricated.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,502,333 to Bertin et al. in View of U.S. Patent No. 5,434,868 to Aichelmann, Jr. et al.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bertin et al. (U.S. Patent No. 5,502,333) in view of Aichelmann, Jr. et al. (U.S. Patent No. 5,434,868). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The nonobviousness of independent claim 8 precludes a rejection of claim 9 which depends therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Aichlemann et al. does not appear to cure the deficiencies in Bertin et al. with respect to claims 8 and 9. Therefore, the Applicant requests that the Examiner withdraw the 35 U.S.C. § 103(a) obviousness rejection to claim 9.

New Claims

Applicants have added new claims 10 through 14, and respectfully submit that same are allowable.

ENTRY OF AMENDMENTS

The amendments to claims 3, 6, 7 and 8 and the addition of new claims 10 through 14 should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Applicants respectfully submit that the amendments effected herein clarify, rather than limit, the scope of the claims with respect to the art of record as presently applied.

CONCLUSION

Claims 1 through 14 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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JAW\csk:dlm
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Enclosure: Version With Markings to Show Changes Made

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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

3. (Twice Amended) A memory module, comprising:

a substrate having a plurality of memory chips individually mounted thereon; and

a programmable device adapted to reroute input and output paths to and from said plurality of memory chips to bypass nonfunctional memory in at least one of said plurality of memory chips, extending to one or more additional individual locations on said substrate and configured to incorporate functional memory of one or more additional chips disposed at said one or more additional individual locations on said substrate into said rerouted input and output paths.

6. (Twice Amended) The memory module of claim 4, wherein said at least one additional memory chip comprises at least two memory chips having different memory capacity and being placed at different additional individual locations.

7. (Twice Amended) The memory module of claim 3, wherein said programmable device comprises [a traffic-control] an EEPROM.

8. (Twice Amended) A memory module comprising:

a plurality of chips individually mounted to a substrate, said plurality of chips collectively exhibiting an amount of nonfunctional memory exceeding a memory capacity of any one chip of said plurality; and

at least one additional memory chip individually mounted to said substrate providing an amount of functional memory equal to or greater than said amount of nonfunctional memory.